Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Q1 Collector**
2. **Q1 Base**
3. **Q1, Q2 Emitter**
4. **Q2 Base**
5. **Q2 Collector**
6. **Q3 Base**
7. **Q3 Emitter**
8. **Q3 Collector**
9. **Q4 Base**
10. **Q4 Emitter**
11. **Q4 Collector**
12. **Q5 Base**
13. **Q5 Emitter**
14. **Q5 Collector**

**.038”**

**.034”**

**1 14**

**2**

**3**

**4**

**5**

**6**

**7 8**

**13**

**12**

**11**

**10**

**9**

**3146**

**MASK**

**REF**

**A**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Substrate Connection: Q5 Emitter**

**Mask Ref: 3146 A**

**APPROVED BY: DK DIE SIZE .034” X .038” DATE: 7/7/22**

**MFG: NATIONAL SEMI THICKNESS .016” P/N: LM3046**

**DG 10.1.2**

#### Rev B, 7/19/02